40nm Embedded Flash Memory Cell Fail Localization for Physical Analysis in 512kB testchip

Applications on erase stress reliability study

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***Abstract*—In this study, memory array of several 512kB testchips are stressed with the worst case erase voltage conditions. Analysis of failed testchips after stress demonstrates failure in the memory array. Therefore specific on-chip characterization are realized to localize the failed memory cells. Physical analysis on these failed cells reveals a potential weakness in the inter-poly oxide conformation. Testchip localization on wafer map reveals a more probable inter-poly breakdown near the wafer borders.**

Embedded Flash memory down scaling leads to dielectric thining, while performance in retention and electric stress wearout are maintained. Understand the cause and conditions of oxide breakdown are fundamental to develop new Flash technology [1]. On-chip characterization brings large statistical data and a product-like approach. Reproducing electrical stress on testschip gives useful insight on the dielectric wear out performance. Specific on-chip characterization, like Direct Memory Access [2], enable to localize spatially failed cells, and to link the electrical failure observed during on-chip characterization with physical failure of the memory cell.

Our testchip consists of a 512kB embedded 40nm Flash Memory disposed on two 256kB NOR arrays. Logic and HV circuit permits to execute Built-in-Self-Test (BIST) in order to read, write and erase the memory. Erase stress is applied using the worst erase voltage conditions during 500s on 100 testchips. After the electric stress, a readout and reconditioning is done to check if the testchip and its memory are still operational.

After stress, reconditioning, 20 testchips are binned to fail state during the readout test. Complete read of the testchip memory state is first done to isolate the failed memory area. A definable feature of this test is a unique page failed. Analysis of voltage generation circuit in the testchip do not show any abnormality. Therefore memory cells integrity have potentially been deteriorated by the electric stress in the given failed memory area.

On Fig. 1 (a), drain current versus voltage measurement are done on all 4096 cells of the failed page by the mean of DMA. Abnormal drain current is found for one cell per page failed. Physical localization of the fails cells in the memory arrays is realized by using the electrical address and the testchip scrambling. Failed testchips with a failed localized memory cell are analyzed by Transmission Electron Microscopy (TEM). In Fig. 1 (b), this physical analysis shows that an inter-poly oxide breakdown occurred between the channel and the control gate at the location where control gate morphology forms a poly tip.

From TEM results, we can assess that the electric field enhanced by the poly tip morphology is surely the cause of oxide breakdown. By analyzing the wafer map of tested chips, we observe a correlation between the probability of fail and testchip localization near the wafer border. Moreover localization of failed memory cells in the testchip array is random, thus not linked to testchip architecture. Hence the poly stack etch process, impacting the poly-tip conformation of the control gate, is not uniform over the wafer and weaken the inter-poly stress resistance at this highlight spot.

To conclude, using specific functions like Direct Memory Access (DMA) coupled with physical analysis of the failed device is very efficient to link testchip electrical failure to oxide breakdown. In this case, insight on inter-poly breakdown is useful to improve process and memory technology reliability.

REFERENCES

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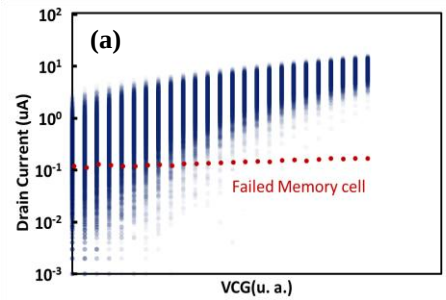

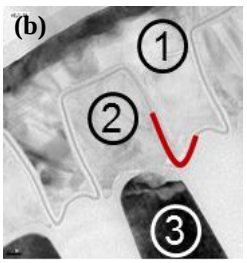

Fig. 1. (a) Drain current measurement of 4096 memory cells of a fail page with a failed cell highlight in red. (b) TEM cut of the failed cells, with the inter-poly breakdown area at the poly-tip in red between the control gate (1), the channel (3) and near the floating gate (2).