High Speed and High-Area Efficiency Non-Volatile Look-Up Table Design Based on Magnetic Tunnel Junction

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Abstract :

Continual growth in the size and functionality of FPGAs over past few years has resulted in an increasing interest in their use for high-speed applications. However, the execution speed is limited by the memory access speed and the whole function is affected due to the great amount of data.

Most FPGAs are implemented with SRAM cells to memorize the chip configuration. However, the drawback of these SRAM cells is their high power consumption and their intrinsic volatility. They constantly need to be powered to store data in stand-by state. Several solutions are thus being investigated to overcome this drawback by introducing emerging non-volatile memory.

In this paper, we focus on the design of a non-volatile Look-Up Table (nvLUT) based on STT-MRAM, which is the core building block in FPGAs. We present a 6-input LUT architecture. The reason behind this choice is that traditional 4- input LUTs have become extremely limited and require several levels of logic to implement complex functions [1]. Many paths were investigated to develop larger LUTs, which have the ability to efficiently implement more than one logic function. However, none of the previous work have achieved a sufficient sensing margin and an acceptable delay performance with wider input Boolean functions.

Our structure's ability allows the possibility to implement arbitrary n-input logic gates. Since the read current path and the CMOS multiplexer tree are separated, the sense delay is reduced by 55 %, the number of MTJs is reduced by 47 %. Additionally the power delay product has a 46% reduction compared to that of the typical structure [2] represented in Fig1. Our proposed circuit ensures a sufficient sense current and a short delay whatever the number of inputs.

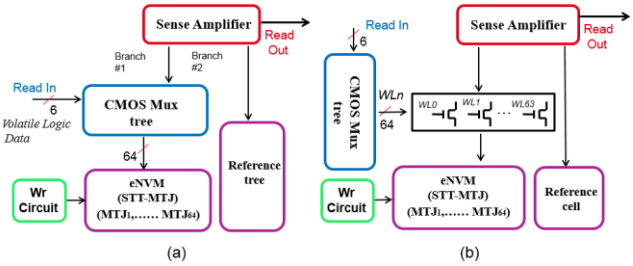

Figure 1. General architecture of a nvLUT. (a) Typical architecture (b) Proposed architecture.

	Sense delay (ps)	
Number of inputs	**Typical circuit**	**Proposed circuit**
3	160	103
4	190	103
6	228	103
8	287	103

Table 1: Sense delay between typical and proposed architectures

REFERENCES

[1] http://www.ni.com/white-paper/7440/en/.

[2] Suzuki, D., et al. "Six-input lookup table circuit with 62% fewer transistors using nonvolatile logic-in-memory architecture with series/parallel-connected magnetic tunnel junctions." *Journal of Applied Physics* 111.7 (2012): 07E318.