High and medium voltage transistors for embedded non-volatile memories on 28nm FDSOI technology

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***Abstract*—High voltage (HV) and medium voltage (MV) transistors are required in integrated circuits with embedded non-volatile memory (eNVM). Most advanced eNVM in production are processed on 40nm nodes. To continue technology scaling and performance enhancement, the integration of HV/MV transistors on thin-silicon body technology (i.e. FDSOI or FinFET) is needed. The main challenges of HV/MV development on 28FDSOI node are presented. Gate stack materials, including deposited oxide and high-k metal gate (HKMG) are discussed and opportunities offered by FDSOI architecture are studied.**

HV ($5V<V_{DD}<11V$) and MV ($3V<V_{DD}<5V$) transistors are needed on eNVM technologies for memory voltage management, analog and I/O functions. The high voltages can be applied either to the drain or gate of the transistor. Thus, a gradual drain/bulk junction as well as a thick and reliable gate oxide are necessary. FDSOI platform introduces several major breakthroughs [1] that strongly impact HV/MV integration. First, the channel of logic transistors operating at low voltage (LV) uses an undoped thin film (7nm) of silicon. To achieve low variability and yield, its thickness is strictly defined and controlled. Also, the traditional poly/SiO_2 stack is replaced by HKMG to increase electrostatic control while lowering the gate leakage.

Gate stack materials is key for reliability and performance. Up to now, HV/MV transistors have used a furnace grown SiO_2 gate oxide associated to a polysilicon gate. Since the SiO_2 layer can be as thick as 15nm, this grown oxide cannot be integrated on a FDSOI platform without increasing process flow complexity. Indeed, the thin silicon film of LV transistors would need a dedicated protection against oxidation. An alternative solution is to use a deposited oxide, high temperature oxide (HTO) being the best candidate [2]. Nevertheless, deposited oxides are less robust than grown oxides and thus need specific treatments to enhance their intrinsic quality. To do so, several processes applied before or after deposition have been investigated including high temperature annealings and limited thermal oxidations. It is demonstrated that HTO with dedicated treatments can meet reliability requirements. Regarding gate stack, a possible integration scheme for HV/MV transistors is to deposit the HKMG directly onto the thick SiO_2 oxide. This solution has been investigated on MOS capacitors. The main detrimental impact of HKMG is the diffusion of Nitrogen from the metal gate towards the gate oxide. This phenomena is responsible for a strong interfacial traps density [3]. However, reliability requirements such as time-dependent dielectric breakdown (TDDB) are still achieved (Fig. 1) making it a suitable solution for HV/MV gate stack.

Advanced nodes also bring new opportunities. FDSOI technology is introduced to overcome short-channel MOSFET limitations. Since it is designed for LV and high performance transistors, HV transistors must use a specific bulk area of the silicon where both thin film and buried oxide are etched. However, MV transistors could benefit from FDSOI architecture and its advantages such as highly efficient back biasing, latch-up immunity [4]... However, hot carrier (HC) degradation is expected to dramatically increase because of strongly pinched channel in fully depleted mode. To ensure reliability, selective thickening of MV transistors channel could be a suitable solution that should be investigated. The possible architecture for LV and MV/HV transistors co-integration is illustrated Fig. 2.

In conclusion, integration of HV and MV transistors on 28nm FDSOI for eNVM purpose must face several challenges. A deposited oxide and a HKMG stack could replace the grown SiO_2/poly stack raising new reliability challenges. For MV transistors, FDSOI architecture can offer new design possibilities if HC degradation can be handled.

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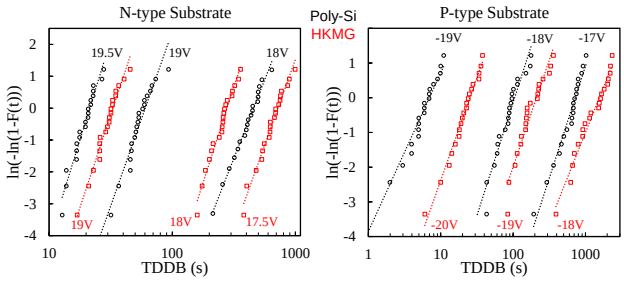

Fig. 1. Comparison of TDDB for Poly and HKMG stack.

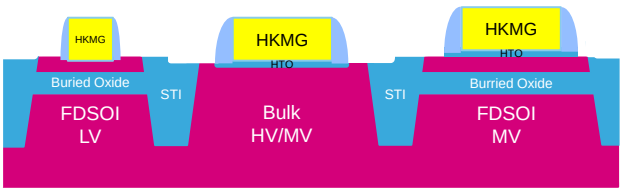

Fig. 2. Logic and HV/MV transistors co-integration.