Bias Voltage Control Cells based on Negative- and Positive Level Shifter Architecture in 28 nm FDSOI Technology

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Abstract:

With the last transistor generations, static power consumption has increased, mainly because of leakage mechanisms in nanometric scale nodes. Recent FDSOI technology is one of the proposed solutions to overcome the Short-Channel Effects (SCE) and to continue scaling down the CMOS circuits. This technology is also well-known for its local body bias effect offering more degrees of freedom to the designers. Indeed, a local dynamic biasing control can be used to increase the power efficiency while enhancing circuit speed. This method requires On/Off-control cells, also called Boost Cells, for locally switching the local body bias voltage. This work analyses and compares 4 different Boost Cells based on Level-Shifter (LS) architectures. The approach not only shows advantages in term of power efficiency but also reduces the required area for the biasing circuitry. The results highlight a significant improvement in term of biasing activation delays between the On/Off-Biasing States and a drastic power consumption reduction.

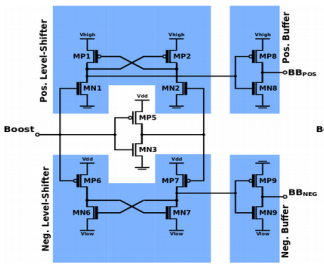

Figure 1: Boost Cell with Conventional LS

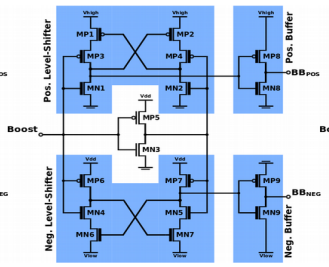

Figure 2: Boost Cell with Contention Mitigated LS

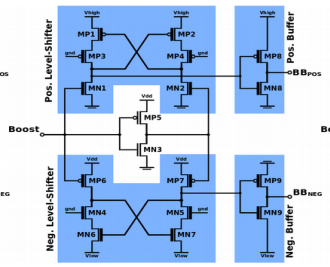

Figure 3: Boost Cell with Iga LS

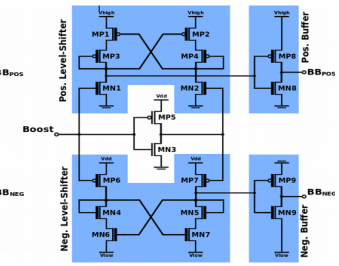

Figure 4: Boost Cell with Reversed Contention Mitigated LS

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