Exploration of magnetic memory for ultra low-power systems-on-chip

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1 Introduction

Memories are currently a real bottleneck to design high speed, low area and energy-efficient systems-on-chip (SoC). An important proportion of total power is spent on memory systems. Ultra low-power (ULP) SoC often use different memory technologies to keep the advantages of each one (area, energy consumption, latency and non-volatility), however there are still penalties and this add more complexity at every development levels.

The permanent need of smaller and consuming less energy SoC (highly requested for Internet of Things (IoT) devices) lead to explore new technologies, architectures and techniques at every levels of the development of these systems.

MRAM (Magnetic Random Access Memory) is seen as a promising alternative solution to replace both traditional SRAM (Static Random Access Memory) and NVM (Non Volatile Memory), thanks to its high density, low read/right latency, non-volatility and negligible leakage current.

Several studies explored the possibilities of MRAM and the combination of MRAM and CMOS to propose fast and low-power memories and new management techniques [2]. However, mostly of these studies focus on high-performance embedded devices, but few focus on ULP SoC where the resources are limited and area and energy consumption are the main issues.

2 Design space exploration of ultra low-power systems-on-chip

Microcontrollers are used in application which are highly constrained by area and power (like a lot of IoT applications). They use to integrate a lot of peripherals needed by the system and so are easier to integrate than microprocessors. Due to the limitations of traditional memory technologies, microcontrollers have both non-volatile memories (mostly FLASH for code in today's generic microcontrollers but other technologies exist), and volatile memory (mostly SRAM).

Dedicated tools make possible the exploration of different kind of memory technologies in a microprocessor at different levels [4] (NVSim [5] for circuit level, gem5 [1] and McPAT [3] for architecture level).

The fact that microcontrollers integrates a lot of modules and peripherals, which their number, their implementation and so their impact on the final system change depending on the manufacturer and the targeted application, makes very hard the development of a unique tool which takes account of all the varieties of microcontrollers.

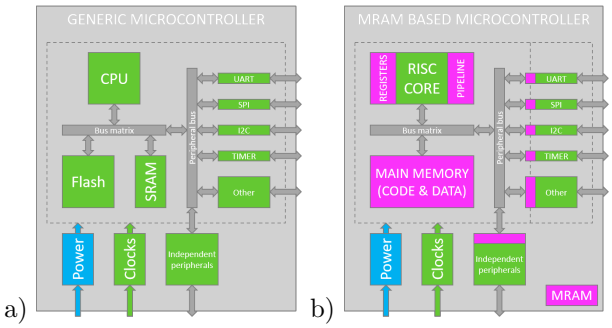

Figure 1. Microcontroller architecture, (a) generic and (b) using MRAM

The aim of this work, part of the MASTA project (MRAM Based Design, Test and Reliability for Ultra-Low-Power SoC), which has received funding from the French National Research Agency under grants ANR-15-CE24-0033-01, is the exploration of MRAM memories in ULP SoC.

References

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