NEURAL NETWORK FOR ULTRA-LOW POWER AND REAL TIME COMPUTATION

Meyer Charly

Université de Bordeaux, IMS laboratory

charly.meyer@ims-bordeaux.fr

My PhD takes place in the AS2N (Architecture on Silicon of Neural Network) team at IMS laboratory (Intégration du Matériaux aux System), which belong to the university of Bordeaux. This work takes part in the ULPEC European project. The main objective of this project is to create a driving assistance device based on neural network thanks to memristors array technology.

During the two last decades, research on neural networks has been significant growth, those neural network are mainly used for recognition and data mining (e.g. Google and YouTube). Their performance for picture recognition are really good, however they need a supercomputer. To limit the power consumption while working in real time, the proposed solution is inspired by the human brain. We have chosen a mixed solution memristive device as synapses, and CMOS to realize neurons.

A memristor is a variable resistance which value changes when a voltage is applied at its terminal. My work is to create and design an electronic neuron on chip to allow read and write the analog memory (memristor).

The neuron[1] is shown in Figure 1. It contains a membrane capacitor, to load any charge who throws memristor, a spike generator who generates a pulse when the membrane voltage reaches a threshold value that one chose. The spike generated allows changing the resistance of the memristor by applying a voltage difference at their terminals.

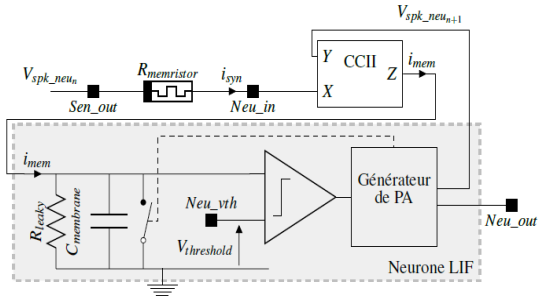

Figure 1: Diagram block of CMOS neuron[1]

To design circuitries I created a memristor's model in Verilog A based on measurements done by our colleagues at Unité Mixte de Physique (UMR CNRS-Thales)[2,3].

For the simulations, several memristors are connected to a postsynaptic neuron. Their conductance defines the gain of the emulated synapses. Each pixel from the input visual sensor is coded by the frequency of spike. To recognize a pattern, neural network need to be trained with some samples. At the end, each output neuron can recognize one pattern.

We have already simulated larger neural network applied on the M-NIST database (hand written numbers) taking into account the variability of memristors. With the best conditions, the recognition rate reached 88.8%[1].

References

1 LECERF, G. (2014). Développement d'un réseau de neurones impulsionnels sur silicium à synapses memristives *Thèse de Doctorat de l'université de Bordeaux*.

2 CHANTHBOUALA, A. et al.(2012) A ferroelectric memristor. *Nature materials, vol 11, October 2012.*

3 BOYN, S. (2017) Learning through ferroelectric domain dynamics in solid-state synapses. *Nature communications, DOI: 10.1038/ncomms14736*|.