Sub-gate Resolution Time-to-Digital Converter based on a Self-timed Ring Oscillator

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Résumé :

Accurate time measurement is a necessity for numerous applications, such as high-energy physics and satellite positioning [1]. This can be carried out with devices called time-to-digital converters (TDCs) implemented mostly with digital elements. The accuracy of a TDC is related to the time resolution by which the measurement is performed. In many architectures, the resolution cannot be lower than the propagation delay of one logical gate [2]. Other architectural techniques with a time resolution lower than the gate delay have been proposed [2, 3]. However, it is very difficult to precisely adjust the time resolution without using complex calibration schemes [4].

In this paper, we present a fully digital TDC based on a self-timed ring (STR) oscillator. In a STR, several events can propagate simultaneously without colliding thanks to a request/acknowledgement handshake protocol. Moreover, the STR presents an accurate time resolution $\Delta\varphi$ which can be tuned as fine as needed by increasing the number of stages [5]. As presented in Fig. 1, a L-stage STR, with a number of events co-prime with the number of stages L, provides L signals evenly distributed over its half oscillation period T_{STR}. Thus, a time base can be generated by equidistant phases with a sub-gate phase resolution. As a consequence, counting the number of edges corresponding to the half period of the oscillation shows that k phases present $M+1$ edge while $L-k$ other exhibit the value M. Hence, the time interval T, which needs to be measured, is expressed as a function of $\Delta\varphi$ and $T_{STR}/2$. knowing that $\Delta\varphi = T_{STR}/2L$, the measured time value T_m is given by (1) which is only function of $\Delta\varphi$: $$T_m = M.\frac{T_{STR}}{2} + k.\Delta\varphi = (M.L + k).\Delta\varphi \quad (1)$$

To validate the proposed method, we have used two different simulation flows on a 28 nm FDSOI technology: analog and high-level timed simulations. An optimized architecture of 9-stage STR-based TDC, initialized with 4 events, has been performed. Simulations show that the measured interval T_m is equal to the *Enable* interval T with an error which does not exceed $2\Delta\varphi$ when the jitter is higher than $\Delta\varphi$. So, on-the-fly measurement on fast non-periodic signals is possible. Conversely, only 52% of the measurements were correct for $\Delta\varphi$ closer to the STR jitter which sets a limit. However, a mean value of many samples can filter this STR noise.

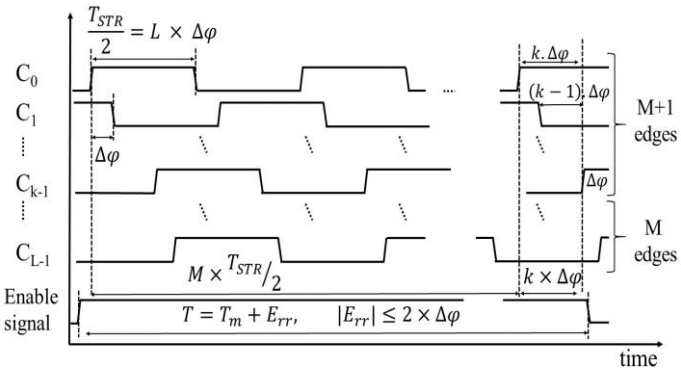

Figure 1 : Time measurement diagram of a L-stage STR

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