InAs/GaSb thin layers directly grown on nominal 300mm (001)-Si substrate by MOCVD for the fabrication of DSA-based InAs NWFET

T. Cerba[1], M.Martin[1], J. Moeyaert[1], B. Salem[1], E. Eustache[1], P. Bézard[1], X. Chevalier[2], G. Lombard[2], S. Labau[1], F. Bassani[1], S. David[1], J.L Rouviere[5], L. Cerutti[4], E. Tournié[4], H. Boutry[3], T. Baron[1]

[1] Univ. Grenoble Alpes, CNRS, LTM, 38000 Grenoble, France
[2] Arkema France, Route Nationale 117, BP34-64170 Lacq, France
[3] Univ. Grenoble Alpes, LETI, 38000 Grenoble, France
[4] IES-CNRS, Univ. Montpellier, 860 Rue St - Priest, 34090 Montpellier, France
[5] INAC-CEA, Univ. Grenoble Alpes, 17 avenue des Martyrs, 38054 Grenoble, France

Contact: tiphaine.cerba@cea.fr

ABSTRACT

III-V are appealing materials as high-speed transistor channels in silicon-based nanoelectronics. InAs and GaSb epitaxial layers grown on silicon substrate are of interest according to their significant electrons and holes mobility, respectively. The device scaling-down depends on the ability to create ever-shrinking dimensions of patterns. Directed self-assembly (DSA)-patterning owing to his period patterns of 10-50 nm length scales is a promising candidate as an alternative patterning method to develop sub-10nm field effect transistor (FET).

In this study we present the electrical, structural and topological characterizations of a GaSb thin layer directly grown on a nominal 300mm (001)-Si substrate. The significant challenge is to deal with crystalline defects, such as dislocations and antiphase boundaries (APBs) induced by the growth of a III-V material on Si substrate with a lattice mismatch of 12%. This GaSb layer packs and minimizes defects density, and so act as a buffer layer for the above-InAs-epitaxial layer. We obtained an APBs-free 250nm GaSb layer on nominal (001)-Si substrate, with a surface roughness RMS as low as 0.6 nm. The X-Ray diffraction measurements revealed a full-width-at-half-maximum (FWHM) of 550 arcsec for a 470 nm GaSb layer which point out a suitable crystalline quality. Electronic microscopy evidenced the presence of a periodic array of 90° dislocations at the interface GaSb/Si and a threading dislocations density of 10^9 cm^{-2} estimated by TEM for a 800nm GaSb layer. Then we pursue with the growth of the InAs epitaxial layer used as channel for an InAs NWFET. In order to obtain densely packed InAs nanowires we deposit topographic Au confinement patterns. To neutralize the affinity of either domain of the PS-*b*-PMMA block copolymer (BCP) with the underlying InAs layer, a ~6 nm-thick brush layer of random PS-*r*-PMMA is spin-coated and thermally grafted to the surface. PS-*b*-PMMA BCP is then spin-coated on top of the stack. The PMMA domain was then removed by a combination of UV exposure and solvent and the brush layer opened by dry-etching[1]. Once revealed, the patterns of the PS mask have been transferred into the underlying InAs sheet[2].

To conclude, we have demonstrated the use of PS-*b*-PMMA to transfer high resolution and high density patterns into a low roughness InAs layer as the first steps towards InAs nanowires. Further publications will introduce the GaSb etch step and the gate-all-around deposition process.

REFERENCES

[1] P. Bézard, Développement de Procédés de Gravure Plasma Innovants Pour Les Technologies Sub-14 Nm...Par Copolymère À Blocs, Grenoble Alpes, 2016.
[2] F. Chouchane, B. Salem, G. Gay, M. Martin, E. Pargon, F. Bassani, S. Arnaud, S. David, R. Alcotte, S. Labau, J. Moeyart, and T. Baron, J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom. **35**, 021206 (2017).